Claims

What is claimed is:

1. A method for implementing a redundancy enhanced differential signal interface comprising the steps of:

detecting an error;

responsive to said detected error, reducing an interface operating speed;

alternately testing of true and complement sides of a differential signaling I/O pair; and

responsive to detecting a failure of a true side or a complement side, setting the detected failed true side or complement side to a reference voltage and maintaining said reduced interface operating speed.

2. A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of detecting said error includes the step of utilizing Error Correction Code (ECC) for error detecting.

3. A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of reducing said interface operating speed includes the step of setting an interface operating speed to about one half of normal operating speed.

4. A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 wherein the step of alternately testing true and complement sides of a differential signaling I/O pair includes the steps of providing a pair of multiplexers coupled to a differential receiver, each multiplexer receiving a respective true or complement signal first input and a voltage reference second input; and each multiplexer providing a respective true or complement output signal to said differential receiver.

5. A method for implementing a redundancy enhanced differential signal interface as recited in claim 4 includes the steps of enabling a multiplexer control for one of said pair of multiplexers; reading data; and checking for the error; and enabling a multiplexer control for the other one of said pair of multiplexers; reading data; and checking for the error.

6. A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 further includes the steps responsive to detecting a failure of both said true side and said complement side, returning to normal operating speed and posting said failure.

7. A method for implementing a redundancy enhanced differential signal interface as recited in claim 1 further includes the steps responsive to detecting no failure of either a true side or a complement side, posting said detected no failure, and continuing operation at said reduced interface operating speed.

8. Apparatus for implementing a redundancy enhanced differential signal interface comprising:

a differential signaling I/O pair;

a differential receiver interface coupled to said differential signaling I/O pair; said differential receiver interface including a pair of multiplexers coupled to a differential receiver, each multiplexer having a first input receiving a respective true or complement signal and a second input connected to a voltage reference and a multiplexer control input; and each multiplexer providing a respective true or complement output signal to said differential receiver;

error detecting means coupled to said differential receiver for detecting an error;

test and failure control logic coupled to said error detecting means and said differential receiver interface; said test and failure control logic being responsive to a detected error, for reducing an interface operating speed; and alternately enabling said multiplexer control input of said pair of multiplexers for testing of true and complement sides of said differential signaling I/O pair; and responsive to detecting a failure of a true side or a complement side, for setting the detected failed true side or complement side to a reference voltage for continued operation.

9. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said test and failure control logic maintains said reduced interface operating speed for continued operation after setting the detected failed true side or complement side to a reference voltage.

10. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said test and failure control logic is responsive to detecting a failure of both said true side and said complement side, for returning to normal operating speed and for posting said detected failure of both said true side and said complement side.

11. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said test and failure control logic is responsive to detecting no failure of either said true side and said complement side, for posting said no failure, and for maintaining said reduced interface operating speed for continued operation.

12. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said reduced interface operating speed is about one half of normal operating speed.

13. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said voltage reference is a middle level voltage between a high and low level of said differential signals.

14. Apparatus for implementing a redundancy enhanced differential signal interface as recited in claim 8 wherein said test and failure control logic tests true and complement sides of said differential signaling I/O pair includes by enabling said multiplexer control for one of said pair of multiplexers; reading data; and checking for the error; and enabling said multiplexer control for the other one of said pair of multiplexers; reading data; and checking for the error.